UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

PATENT NO. : 6,764,901 B2

: July 20, 2004

DATED INVENTOR(S) : Noble et al. Page 1 of 3

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title page,

Item [56], References Cited, OTHER PUBLICATIONS,

- "Askin, H.O., et al.," reference, after "Parameters" delete "for".
- "Foster, R.," reference, delete "et a." and insert -- et al. --, therefor.
- "Hodges, W.T., et al.," reference, after "section" insert --: --.
- "Kishimoto, T., et al.," reference, delete "14" and insert -- 34 --, therefor.
- "Kohyama, Y., et al.," reference, delete "Honoluly" and insert -- Honolulu --, therefor.
- "Kohyama, Y., et al." reference, insert -- (-- before "Jun.".
- "Koshida, N., et al.," reference, delete "Photoluminesceence" and insert
- -- Photoluminescence --, therefor.
- "Masu, K., et al.," reference, delete "Metallizatin" and insert -- Metallization --,
- "McCredie, B.D., et al.," reference, delete "462" and insert -- 461 --, therefor.
- "Ott, A.W., et al.," reference, delete "A1303" and insert -- AI303 --, therefor.
- "Saito, M., et al.," reference, delete "Honoluly" and insert -- Honolulu --, therefor.
- "Senthinathan, R., et al.," reference, delete "Parasite" and insert -- Parasitics --, therefor.
- "Terauchi, M., et al.," reference, delete "1991" and insert -- 1993 --, therefor.
- "Verdonct-Vandebroek, S., et al.," reference, delete "Verdonct" and insert
- -- Verdonckt --, therefor.
- "Wang, P.W., et al.," reference, delete "Characterization" and insert -- Characteristics --, therefor.
- "Su. D., et al.," reference, delete "Signal- Integrated" and insert -- Signal Integrated --, therefor.

Column 1,

Line 37, delete "an" and insert -- a --, therefor.

Column 2,

Line 50, after "trench" insert -- . --.

Column 6,

Line 32, after "depicted here." delete "Each memory cell is constructed in a similar manner. Thus, only memory cell 202C is described herein in detail. Memory cell 202C includes pillar 204 of single crystal semiconductor material, e.g., silicon, that is divided into first source/drain region 206, body region 208, and second source/drain region 210 to form access transistor 211. Pillar 204 extends vertically outward from substrate 201 of, for example, p- silicon. First source/drain region 206 and second source/drain region 210 each comprise, for example, n+ silicon and body region 208 comprises P-silicon"

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Column 6 (cont'd),

and insert -- Each memory cell is constructed in a similar manner. Thus, only memory cell 202C is described herein in detail. Memory cell 202C includes pillar 204 of single crystal semiconductor material, e.g., silicon, that is divided into first source/drain region 206, body region 208, and second source/drain region 210 to form access transistor 211. Pillar 204 extends vertically outward from substrate 201 of, for example, p- silicon. Fast source/drain region 206 and second source/drain region 210 each comprise, for example, n+ silicon and body region 208 comprises P- silicon. -- as a new paragraph on line 33.

Column 7,

Line 1, delete "late" and insert -- plate --, therefor.

Column 8,

Line 49, delete "322" and insert -- 332 --, therefor.

Column 9,

Line 3, delete "322" and insert -- 332 --, therefor.

Column 11,

Line 58, delete "claim 13" and insert -- claim 16 --, therefor. Line 61, delete "claim 13" and insert -- claim 16 --, therefor.

Column 16,

Lines 52 - 53, after "the top" delete "even with the top".

Column 17,

Line 28, after "substrate," delete "a".

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Page 3 of 3

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Column 18,

Line 3, after "top" delete "even with the top".

Signed and Sealed this

Twenty-second Day of February, 2005

JON W. DUDAS Director of the United States Patent and Trademark Office